



iMS4-P -xxx (revD)

Modular Quad Output Synthesizer

Overview and Basic Operation

Models -

Model	Outputs	Feature	Max Frequency Range (MHz)	RF Output Power
iMS4-P	4	Standard model with USBII, III and GbE	10 – 210MHz	1.2mW

Enhanced version of the rev-C including:

- increased data rate to ~ 4MHz.
- programmable delay between input clock and RF output.
- fast digital sync outputs with invert option.
- mixed digital sync outputs; constant level or programmable width pulse per image point.
- independent timing between output channel pairs for X-Y AO scanning applications.

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Supporting Documents: <https://isomet.com/ManImsFun.html>

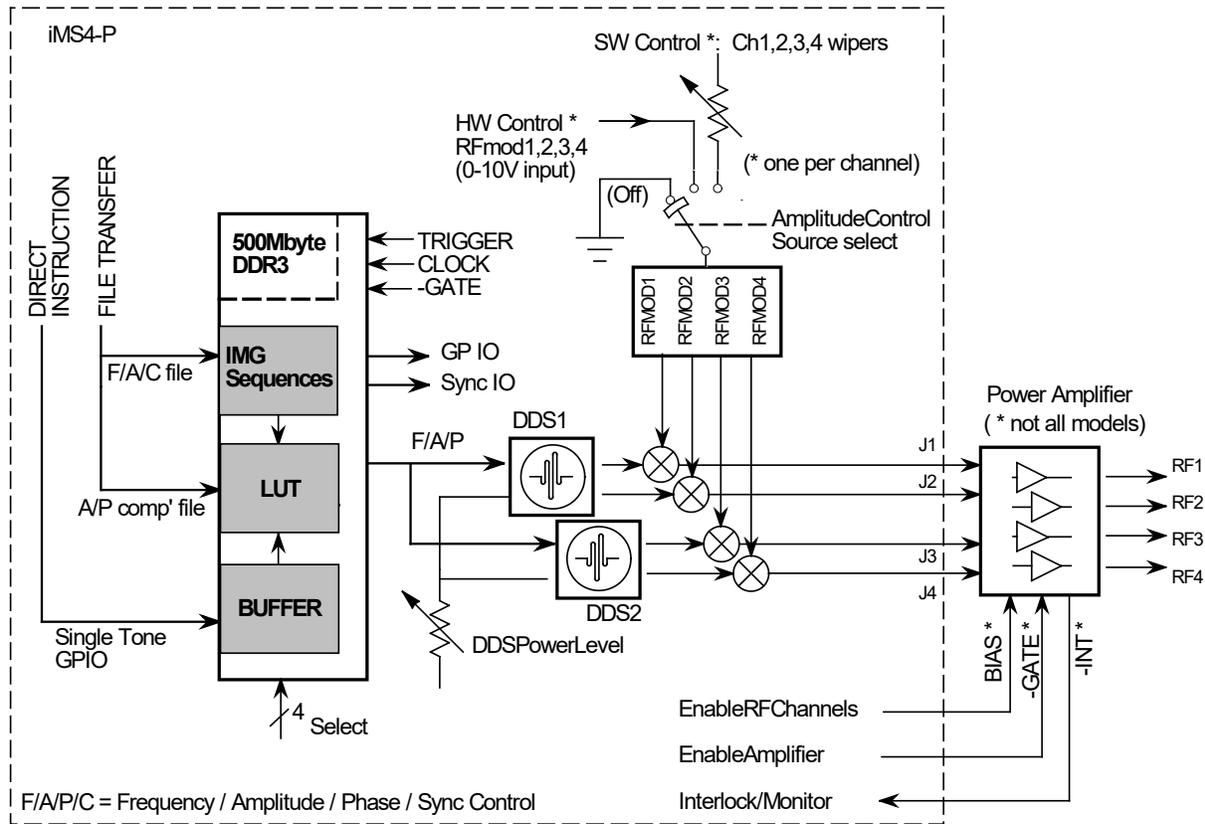
Note: documents specifically describing rev-C will also apply to rev-D usage and applications

Recommend-

- AN220207: External Signal Input Levels
- AN231108: Input_ Output Timing and Programmable Delays rev-D
- AN210323: Isomet Studio - Running Image mode example
- AN210414: Isomet Studio - Running Tone Buffer example
- AN230606: Isomet Studio GUI Overview
- Isomet App Note AN220110: Ethernet Connection and IP setting

1. Hardware Overview and Key features.

The diagram below is a basic schematic of the iMS4-P (rev-D) connected with a generic Power Amplifier. **Before** operating the IMS4-P, it will be necessary to load the USB Window drivers. (See section 10). The IMS4-P operates from DC power and requires a 15V-24Vdc supply (0.5A at 24Vdc)



The iMS4 synthesizer features three basic operating modes -

1.1 Local Tone Buffer (LTB) or Single Tone Mode.

This mode is useful for setting the AO Bragg Angle or switching rapidly between 256 preassigned points. The DDS synthesizer generates a single tone output at the specified Frequency, Amplitude and Phase triad. (Abbreviation F/A/P).

Key features:

- Up to 95 KHz update rate.
- The required output tone may be selected via software control or from hardwired inputs.
- Option to bypass the LUT modifier (see LUT description below).



1.2 IMAGE or Sequence mode.

This mode is useful for generating complex scan patterns at high data rates.

Image files containing the desired frequency scan patterns are downloaded into memory space within the iMS4-P. Output play back is under the control of Trigger and Clock signals provided from an external system or internally generated.

Key features:

- Update rate up to 3.5MHz, (application dependent).
- Any frequency pattern may be generated e.g. random, linear, step, saw tooth.
- Multiple frequency images can be uploaded, images sequences created, appended, deleted and output order modified.
- Simultaneous upload and play of image files.
- Very large image size, in excess of 10million frequency points.

Image and Compensation LUT files (calibration files) can be generated with the supplied GUI, the C++ SDK or on Excel Spread sheet and imported into the C++ project.

1.3 Enhanced tone mode (Ramp / Step mode)

This mode uses the inherent sweep functions built into the DDS chip.

Frequency OR amplitude can be ramped in value.

Note: There is no dynamic control of phase or amplitude during a frequency sweep or chirp.

The amplitude level remains constant during a frequency sweep duration. There is no phase control, so the benefits of using the Compensation LUT function (= AOD beam steering) cannot be applied.

1.4 Control Features

- **Look-up-table (LUT)**

A calibration or compensation look-up-table (LUT) contains frequency specific phase and amplitude data. Its purpose is to compensate for non-linearity and non-uniformities in the wider system.

E.g. create efficient uniform intensity scan lines in an AOD base laser scanning system.

Initial values for the LUT are calculated and loaded into the IMS prior to running the Local Tone Buffer or Image modes. Subsequently, LUT values may be modified with real world measured data or integrated within a feedback mechanism.

- **Point Amplitude control.**

Each frequency point is assigned a unique 10-bit amplitude value ranging from 0 -100% of the maximum RF power setting. This is a relative value and is dynamic i.e. able to change from output point to output point.



- **Static Power Level control.**

The maximum RF output power setting is defined by *UpdateRFAmplitude* and *UpdateDDSPowerLevel* functions via digital potentiometers. These are 8-bit static controls and together define the absolute RF power level of the IMS4-P (and any connected power amplifier module).

- *UpdateDDSPowerLevel* applies to all four channels simultaneously.
- *UpdateRFAmplitude* is channel scoped. Each channel can have a different value.

- **Auxiliary Digital and Analog I-O signals**

The IMS4-P also features:

<u>Signal Description</u>	<u>Ident</u>
12 bit Synchronous output register, updated with the each new image point,	SDOR[0...11]
4 bits Asynchronous output,	GP Out[1...3]
8 bits Asynchronous input,	GP In[1...8]
1 bit 24V PLC compatible opto-relay output,	'Laser' bit
4 pairs RS422/encoder differential inputs	ENC [(A-P, A-N)...(C-P, C-N)]
2x Synchronous analog outputs, 0 - 2.5V full scale	AOUT_Frq ...Amp
1x Asynchronous analog output, 0 - 5V full scale	AOUT_DAC
2x Asynchronous analog inputs, 0 -10V full scale	Aux_ADC1 ... 2

2 Main operating modes and functions.

Please refer to the application program interface (API) documentation with the software development kit (SDK) available as a download.

2.1 Single (Set Calibration) Tone.

Simplest mode.

Direct programming of the DDS frequency, amplitude and phase values.

Bypasses LUT compensation.

2.2 Local Tone Mode

The Local tone buffer (LTB) area contains a maximum 256 F/A/P locations.

The 256 F/A/P Tones may be rapidly addressed using 8x external LTB address lines or directly from the operating software.

LTB ext'l address, J8 (pins 3,4,5,6,16,14,7,8).	Function	Update rate
0 h ... FF h	Select Tone address	10.5usec

The compensation look-up-table (see below) may be applied to the Tone Buffer output if required.

2.3 Enhanced Tone Mode (Ramp / Step mode)

This mode uses the inherent sweep functions built into the DDS chip allowing frequency, amplitude or phase to be ramped in value. However, an internal limitation in the DDS chip prevents amplitude ramps in the Enhanced tone mode. Therefore, only frequency ramps and steps will be described.

2.3.1 Ramp Mode

A ramp or chirp is generated by rapidly incrementing the frequency. The number of increment steps and duration of the ramp are user programmable. Each output can be programmed with different ramp parameters.

The ramps are initiated from the GUI or applying a signal to the external Profile inputs on connector J7.

Available functions:

- Independent Up - Down ramp slopes.
- Dwell (stop at end value) or no-dwell (return to start value) at end of sweep duration.
- Set amplitude value for ramp. (remains constant for the ramp duration).

The Ramp mode offers the fastest frequency sweep capability, with a minimum dwell time of 8nsec per frequency increment.

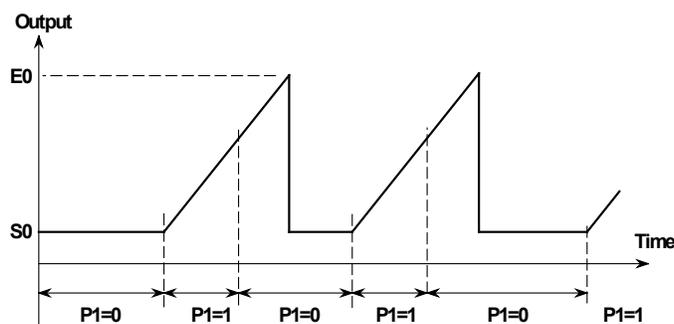
Independent sliders for each of the four output channels define:

- Duration of the rising slope increment.
- Duration of the falling slope increment.
- The number of points for each ramp, up or down.

The falling slope only applies if 'Dwell' is selected in the **Mode** pull down menu.

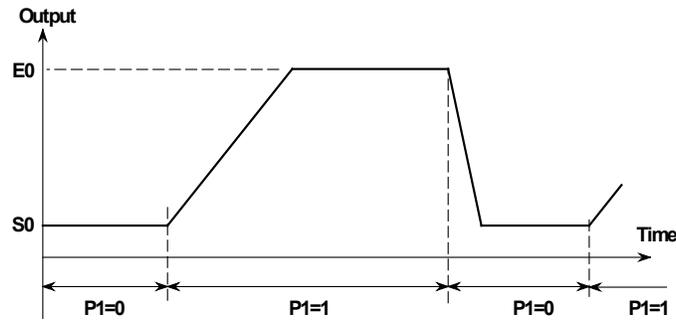
A **Frequency Sweep no dwell** immediately returns to the start value after the end value has been reached

A **No-Dwell** sweep immediately returns to the **Start** slider value (S0) after the **End** slider value (E0) has been reached.



A **Frequency Sweep Dwell** only returns to the start value after a falling edge transition on the appropriate profile input.

A **Dwell** sweep only returns to the **Start** slider value (S0) after a falling edge transition on the appropriate profile input.

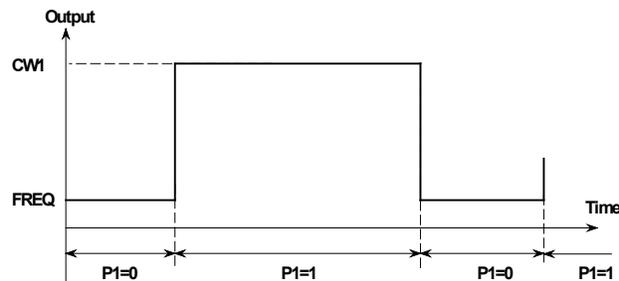


Both plots show a ramp on output J2, controlled using input P1 (on connector J7).

2.3.2 Step mode

This is essentially a two-level sweep or two-level modulation. Step mode may be applied to the Frequency, Amplitude or Phase. Dwell/No dwell has no function.

Plot shows a frequency step sweep for output J2 controlled using input P1.
 FREQ = Start Value
 CW1 = End Value



2.3.3 Amplitude

The amplitude level across a Frequency or Phase sweep (or step) remains a constant. The value is set by a combination of the **DAC Current** level buttons (Full, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$) and the sliders on the **Signal Path** panel.



3 Image Mode.

An Image contains multiple F/A/P data points pre-arranged to give the desired frequency or scan pattern. Image playback is initiated with the Image Trigger. The output update rate is determined by the Image Clock. The Image trigger and clock may be software generated or applied from external sources. At each clock edge, the next location in the Image Memory area is addressed. The frequency and amplitude data point are read and modified by the LUT data (see below). The resultant F/A/P triad is routed to the DDS registers. An update clock is then issued to the DDS and all 4x RF outputs are simultaneously updated* with a new Frequency, Amplitude and Phase value. Any programmed Synchronous control data will also be updated on the appropriate I/O port.

Multiple images can be grouped together into a play sequence. Each image within a sequence can have unique properties such as clock rate and post image delay. Likewise multiple sequences can be defined and queued. These are uploaded into the iMS DDR memory and played in FIFO order. Memory is dynamically allocated to permit flexibility in the size and number of both the images and sequences, and to allow simultaneous upload and output of data. The total number of images (excluding repeats) is 4096. The size of a single image is in excess of a 1million F/A/P points.

4 Look-up-table (LUT).

The LUT is frequency-addressed look-up-table for applying amplitude and phase compensation to the RF signal output. The tables are indexed by the nearest programmed LUT frequency to the demanded output frequency. Table entries are linearly spaced in frequency from the lowest to highest supported. The number of entries in the table is hardware specific. At a minimum, the LUT must contain amplitude compensation data over the desired frequency range of interest.

LUT Size: 2047 entries equally spaced from 10 – 225MHz.

Primary features: Frequency dependent compensation data:

- Amplitude: a value between 0 and 100% for modifying the output amplitude according to frequency. Used for compensating variations in AO efficiency and/or power amplifier gain.
- Phase: 0 - 360 degrees. Value represents the phase offset between adjacent channels. Typically applied to beam steered (= phased array) AO deflector designs. Channel 1 is the reference and unmodified. Channel 4 will exhibit the largest phase differential relative to Ch 1.

Secondary features: Synchronous output data:

- Sync Analog: A value between 0.0 and 1.0 that can be output on one of the synchronous DAC outputs (J7). Updated in step with the specified output RF frequency(s).
- Sync Digital: A binary value that can be output on the synchronous digital outputs. Updated in step with the specified RF output frequency(s).

(* disregarding Image Clock Delay function)



In both cases, the LUT can be bypassed if required. The LUT is applied by default.

6 Technical Specifications.

Image Mode

Timing	Value	Condition
Frequency Settling Time	One cycle at output frequency.	Step change in Image data value. Phase accumulator re-sync = OFF (default)
Frequency Settling Time	< 40nsec	Step change in Image data value Phase accumulator resync = ON Initiated every clock update
Pipeline delay: Image Clock to output	1.2usec	
Minimum Trigger to Clock edge	10 nsec	
Maximum Image Clock rate	2.6 MHz	Dual axis AOD applications (4MHz in development)
Minimum Image Clock rate	0 Hz	

GATE, TRIGGER, CLOCK inputs. J9, J10, J11	Value	Condition
Absolute Maximum Input Voltage	5.5V	Per input.
Recommended Input Voltage	3V < Vh < 5V	Vh = Logic High
Minimum Input Voltage	0V	

Active edge of the external Clock or Trigger inputs is user programmable. Default = rising

Local Tone Buffer Mode

Timing	Value	Condition
Frequency Settling Time		See Image mode values
Output Delay - LTB address change	6usec	
Maximum LTB address rate	95KHz	
Minimum LTB address rate	0 Hz	

+

LTB address, input Voltages, J7	Value	Condition
Absolute Maximum Input Voltage	5.5V	Per input.
Recommended Input Voltage,	3V < Vh < 5V	Vh = Logic High
Minimum Input Voltage	0V	
Isolated, signal source sink current	4mA	Per input

External Modulation Inputs, J7

Parameter	Value	Condition
RF output Rise time	< 40nsec	Step change in external modulation input
Output Delay - Modulation input	50nsec	Step change in external modulation input
Absolute Maximum Input Voltage	12V	Per input.
Recommended Input Voltage	10V	
Minimum Input Voltage	0V	
Input impedance	~600Ω	Per input
On:Off ratio	> 35dB	Full range
Maximum modulation rate	10MHz	
Minimum modulation rate	0 Hz	

RF power control, SDK

Max – Min	Full Range	Condition
DDS Power Level	~ 8dB	All other variables at max power
Amplitude Control Source : Ch-Wiper or Ext'l input	39dB	
Image Point or Tone Buffer Amplitude data	48dB	10bit range
LUT Amplitude Data	48dB	10bit range

RF outputs, J1,J2,J3,J4

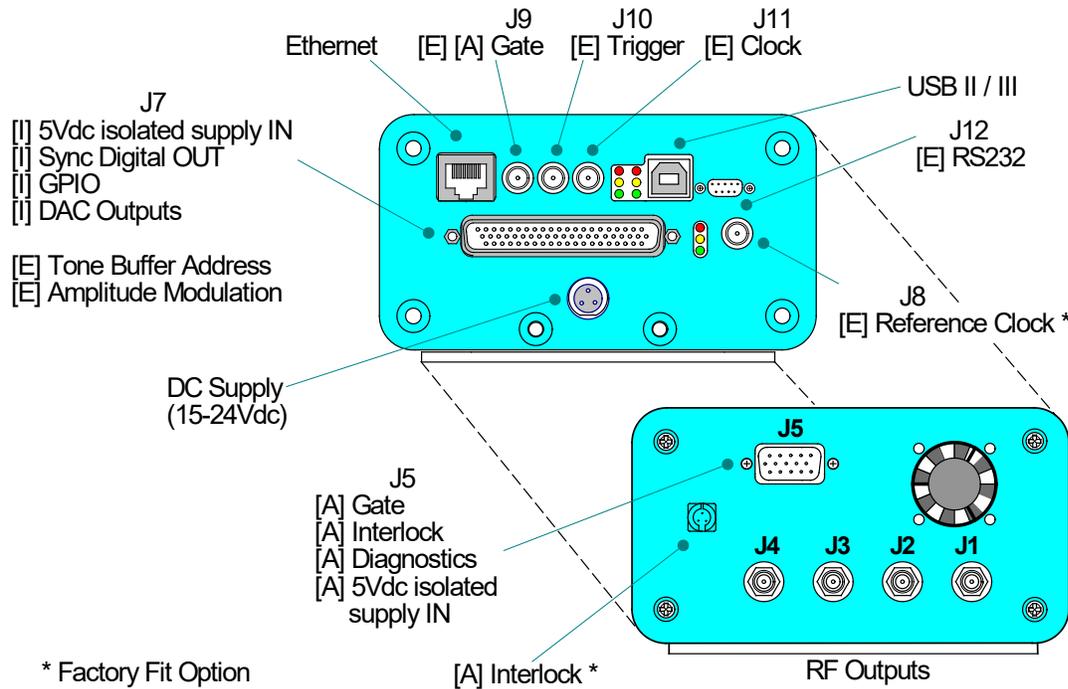
RF Output	Full Range	Condition
Maximum frequency range	10-225MHz	
Recommended frequency range	20-200MHz	
Maximum output power	> 1.2mW / 0.8dB	at 80MHz
Frequency Stability	+/- 2.5ppm	-40C to +85C
Spurious output	> 40dBc	
Harmonics	> 40dBc	at 0.5mW output
Channel to Channel Isolation	> 47dB	at 1mW output

Typical output levels at 110MHz, peak-peak voltage, **50ohm** termination (0.64Vpp=1mW=0dBm)

		Ch1,2,3,4 Level (or relative external modulation level)										
		0%	10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
DDS Level	0%											
	10%	0.008	0.009	0.02	0.05	0.10	0.15	0.18	0.21	0.22	0.24	
	20%	0.008	0.010	0.02	0.07	0.12	0.17	0.20	0.23	0.24	0.25	
	30%	0.009	0.013	0.02	0.07	0.12	0.18	0.21	0.23	0.25	0.27	
	40%	0.009	0.014	0.03	0.08	0.13	0.18	0.22	0.25	0.27	0.28	
	50%	0.009	0.014	0.03	0.08	0.14	0.19	0.24	0.27	0.29	0.31	
	60%	0.009	0.014	0.03	0.09	0.16	0.22	0.26	0.29	0.32	0.33	
	70%	0.010	0.015	0.04	0.10	0.17	0.24	0.30	0.33	0.35	0.37	
	80%	0.011	0.017	0.05	0.11	0.20	0.27	0.34	0.38	0.42	0.44	
	90%	0.013	0.025	0.06	0.15	0.23	0.32	0.42	0.48	0.52	0.55	

	100%	0.017	0.050	0.11	0.20	0.34	0.46	0.56	0.65	0.72	0.76
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7 Hardware Connection.



Minimum Connections:

- USB II / III or Ethernet to a host PC.
- DC Supply, 15V / 2A minimum to 24V / 1.0A maximum
- One or more RF outputs, as required.

Recommended channel connections

AOD / Amplifier Channels	ims4 Outputs
Single	Any
Dual	J1, J2 or J3, J4
Quad	All, in ascending or descending order

Optional connections are identified as follows:

- [E] = hardwired control signals from external signal source(s). Functionally equivalent software generated control signal are provided in the SDK.
- [I] = opto-isolated IO buffered signals requiring an external 5Vdc supply connection to J7
- [A] = external power amplifier connections (see explanation below)



The iMS4-P features external power amplifier diagnostic and control signals. These are available on J5. J5 will require a 5V DC feed for the opto-isolator supply (5V_RFA) provided by the connected RF amplifier. An appropriate interface card must exist within the power amplifier.

8 Power Amplifier Control

The iMS4 allows control and diagnostics functions for connected equipment fitted a suitable interface.

- **Enable/Gate Control**

With few exceptions, most Isomet existing power amplifier modules require an active low Gate or Enable signal to operate and will output a normally closed over-temperature thermal interlock signal.

- **Diagnostics**

Certain amplifier models feature diagnostic outputs including:

- Forward and reflected RF power (between the PA outputs and connected AO device/load).
- Temperature of the PA
- DC current
- Temperature of the AO device

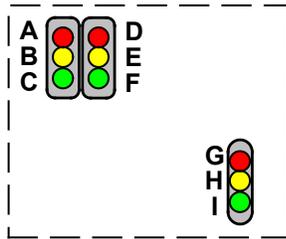
These are communicated via I2C bus on J5 .

Examples include:

Model	Channels	Power/ch	Frequency Range	Enable/Gate Control	Diagnostics
500C- series	1	2,4, or 7W	Model dependent	NA	NA
AFO- series	1	4 or 7W	Model dependent	NA	NA
AG0- series	1	1W	Model dependent	NA	NA
AJ0- series	4	12 or 25W	Model dependent	J5	NA
RFA200-2H	2	100W	35 – 65	J5	NA
RFA1170-4	4	80W	48-92	J5	J5
RFA0110-x-20	2	20W	90-130	J5	J5
RFA0120-x-15	4	15W	100-140	J5	J5
RFA0140-x-12	4	12W	120-160	J5	J5

NA= not applicable

9 LED Indicators.



Top Stack, Controller PCB

Ident	LED	Mode	iMS4-P
A	RED (top left)	If illuminated	Not Downloading File
B	Yellow	If illuminated	Downloading File
C	Green	Pulsing	Controller OK
D	RED (top right)	If illuminated	Image output stopped
E	Yellow	If illuminated	Waiting on Trigger
F	Green	If illuminated	Image playing / output active

Lower stack. Synthesizer PCB

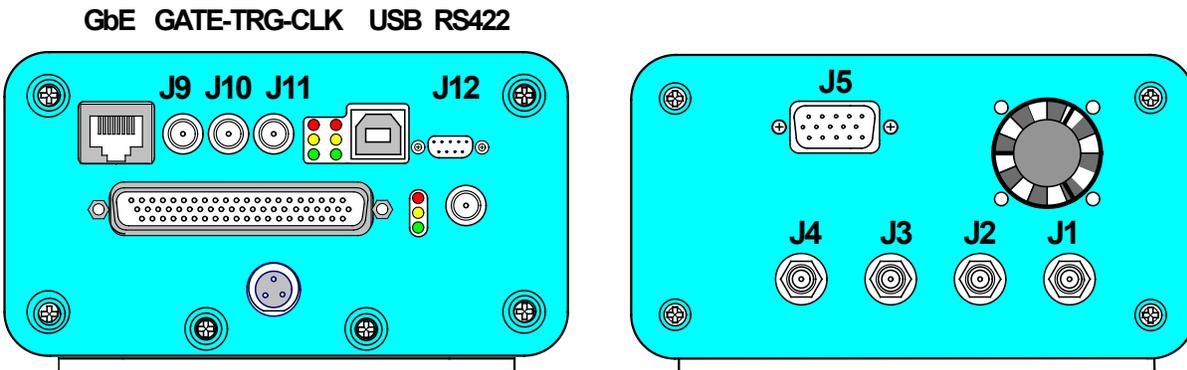
Ident	LED	Mode	Stand Alone iMS4-	In combination with amplifier with J5 connected
G	RED (top)	Constant on	DC power On	Thermal Interlock Open (= fault) <u>or</u> Gate input (J9) not active or nc
H	Yellow	Constant on	NA	PA is enabled. Thermal Interlock OK
I	Green	Pulsing	Synthesizer OK	Synthesizer OK

DC power applied, USB communication problem

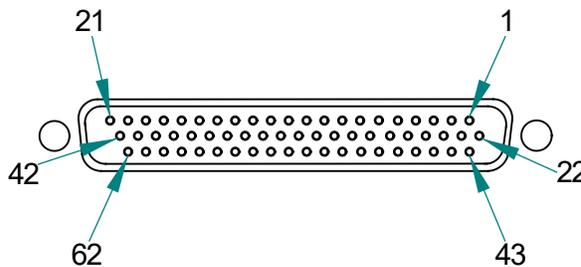
If the 6x LED's (A,B,C,D,E,F) are constantly illuminated, then USB communication has not been established. In this case:

- a: Ensure USB driver is loaded (see section 10)
- b: Cycle DC power
and /or
- c: Disconnect then reconnect USB

10 Connector pinouts.



D-type pin idents looking into the female 62-way connector on iMS4

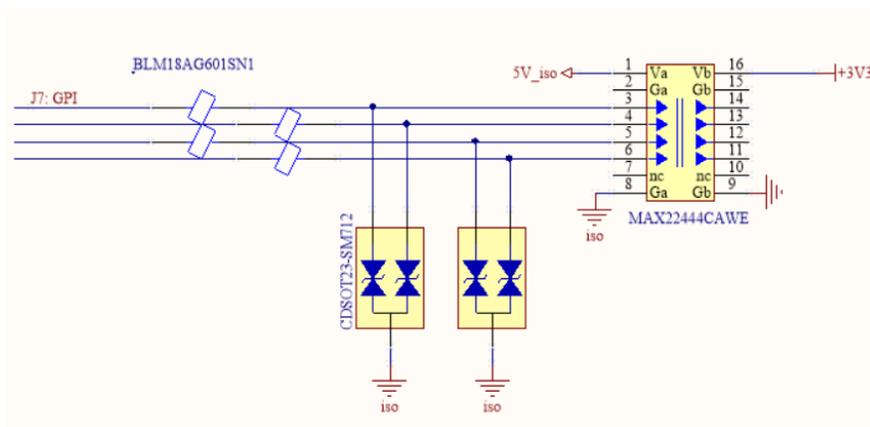


Pin-out descriptions as follows:

Circuit details for isolated inputs / outputs on J7 connector

Input high voltage >3.5V, Input low voltage <0.8V

Input circuit for opto-isolated logic inputs e.g. GPI and Profile



Opto-isolated logic output schematic

Output high voltage <math><4V</math>, -4mA max, Output low voltage <math><0.4V</math>, 4mA max

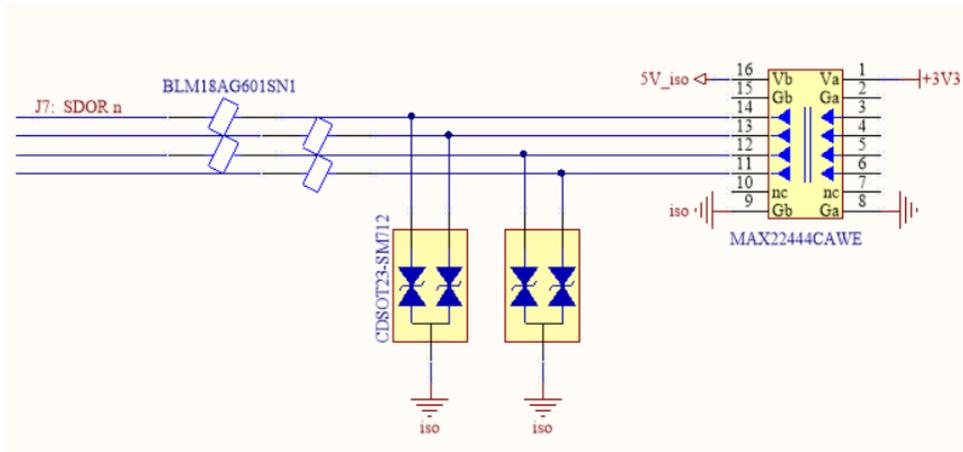
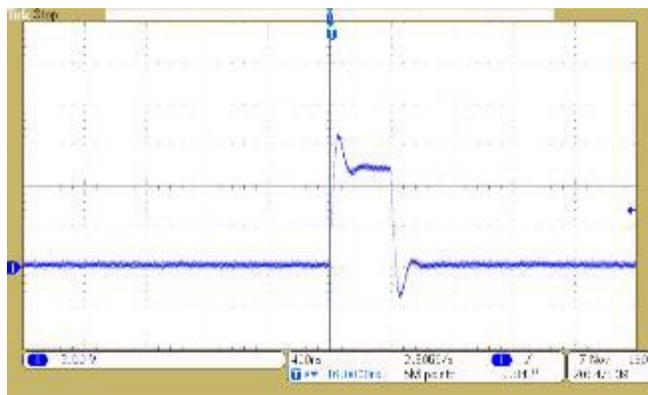


Diagram shown with outputs to J7 on left

SDOR output trace at 2.5MHz Image clock rate

SDIO bits 0..11 are actively driven high. No pull-up resistor required.

DO NOT short outputs to 0V or 5V





Connector	Type Ident	62way HD-D J7	(Continued)		
Signal Designation	Signal	Type	Description	Alternate use	Pin
5V_iso	DC		Isolated 5V DC supply input	5V output, 10mA	44
5V_iso	DC		Isolated 5V DC supply input	5V output, 10mA	24
D_Rtn	DC		isolated 0V / signal return input	0V	25
SDOR0	Out	isolated logic	Synchronous-Digital Output bit0		51
SDOR1	Out	isolated logic	Sync-Digital Output bit1		50
SDOR2	Out	isolated logic	Sync-Digital Output bit2		49
SDOR3	Out	isolated logic	Sync-Digital Output bit3		34
SDOR4	Out	isolated logic	Sync-Digital Output bit4		56
SDOR5	Out	isolated logic	Sync-Digital Output bit5		57
SDOR6	Out	isolated logic	Sync-Digital Output bit6		58
SDOR7	Out	isolated logic	Sync-Digital Output bit7		59
SDOR8	Out	isolated logic	Sync-Digital Output bit8		36
SDOR9	Out	isolated logic	Sync-Digital Output bit9		52
SDOR10	Out	isolated logic	Sync-Digital Output bit10		53
SDOR11	Out	isolated logic	Sync-Digital Output bit11		38
D_Rtn	Out		isolated 0V / signal return input	0V	31
D_Rtn	Out		isolated 0V / signal return input	0V	35
ENC_D_N	In	5V differential logic	Encoder Input N, Channel D		10
ENC_D_P	In	5V differential logic	Encoder Input P		11
ENC_C_P	In	5V differential logic	Encoder Input P, Channel C		12
ENC_C_N	In	5V differential logic	Encoder Input N		13
ENC_B_N	In	5V differential logic	Encoder Input N, Channel B		14
ENC_B_P	In	5V differential logic	Encoder Input P		15
ENC_A_P	In	5V differential logic	Encoder Input P, Channel A		16
ENC_A_N	In	5V differential logic	Encoder Input N		17
D_Rtn	In	(5V iso supply required)	isolated 0V / signal return input	0V	33
GP O1	Out	isolated logic	Async general purpose output		6
GP O2	Out	isolated logic	Async general purpose output		7
GP O3	Out	isolated logic	Async GP logic output		8
GP O4	Out	isolated logic	Async GP output		9
D_Rtn	Out		isolated 0V / signal return input		27
24V_laser	In	PLC	Laser Opto-Supply		60
Laser_Bit	Out	PLC	Laser Opto relay bit Tr/Tf < 50usec)		61
Gnd_laser	In	PLC	Laser Opto-Gnd		62
AOUT_Frq	Out	Analog	8-bit analog representation of Image freq		40
AOUT_Amp	Out	Analog	8-bit analog equivalent of Image amplitude		42
A_Rtn	Out	Analog	Analog return		41
AOUT_DAC	Out	Analog	GP 12-bit DAC analog output.		19
A_Rtn	Out	Analog	Analog return		18
Aux_ADC1	In	Analog	GP Analog input. 12-bit ADC (0 to 10V).		21
A_Rtn	In	Analog	Analog return		(18)
Aux_ADC2	In	Analog	GP Analog input. 12-bit ADC (0 to 10V).		20
Notes:				Key:	
Type Logic = TTL or 5V CMOS				GP = General Purpose	
Factory option: non-isolated logic				LTB = Local Tone Buffer	
(xx) shared pin				nc = not connected	



Other Connectors

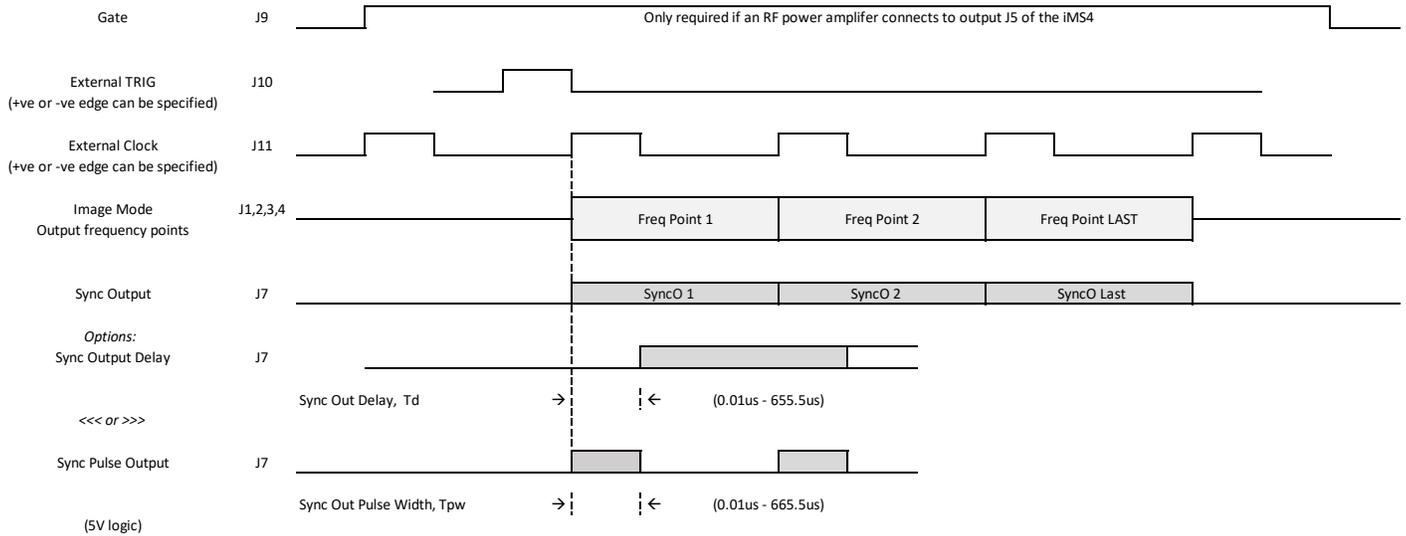
Signal Designation	Signal	Type	Description	Alternate use	Connector	Ident	Pin
Communication							
Ethernet	In/Out	Logic	GbE		RJ45		
USB Serial	In/Out	Logic	USB II / USBIII		B-type	-	
RX-P	In	Logic	RS422 receive+		9-way D	J12	2
RX-N	In	Logic	RS422 receive-		9-way D	J12	1
TX-P	Out	Logic	RS422 transmit+		9-way D	J12	7
TX-N	Out	Logic	RS422 transmit-		9-way D	J12	6
Rtn	Gnd		Sig Rtn		9-way D	J12	5
DC Supply							
Vdc	DC	DC-In	Supply 15V -24V dc, <0.4A		3w TINI-Q		1
	0V	DC-In			3w TINI-Q		2
SMA Coax Connections							
Gate	In	Logic	Enable power amplifiers via J5	POF input	SMA coaxial	J9	Centre
Rtn	Gnd		Sig Rtn				Outer
Trigger	In	Logic	Trigger Image Data Output	POF input	SMA coaxial	J10	Centre
Rtn	Gnd		Sig Rtn				Outer
Clock	In	Logic	Clock Image Data	POF input	SMA coaxial	J11	Centre
Rtn	Gnd		Sig Rtn				Outer
Ch0	Analog	RF	RF1 frequency output, 50Ω		SMA coaxial	J1	Centre
Rtn	Gnd		Sig Rtn				Outer
Ch1	Analog	RF	RF2 frequency output, 50Ω		SMA coaxial	J2	Centre
Rtn	Gnd		Sig Rtn				Outer
Ch2	Analog	RF	RF3 frequency output, 50Ω		SMA coaxial	J3	Centre
Rtn	Gnd		Sig Rtn				Outer
Ch3	Analog	RF	RF4 frequency output, 50Ω		SMA coaxial	J4	Centre
Rtn	Gnd		Sig Rtn				Outer
(Factory fitted option or nc)							
Clock	In	20dBm/50ohm	Reference Clock		SMA coaxial	J8	Centre
Rtn	Gnd		Sig Rtn				Outer
J5 Power Amp Control *							
5V_RFA	In		Opto supply from connected PA	5V, 20mA out	15w-HD D	J5	1
5V_RFA	In		Opto supply from connected PA	5V, 20mA out	15w-HD D	J5	10
0V_RFA	In		Opto 0V from connected PA	0V	15w-HD D	J5	4
0V_RFA	In		Opto 0V from connected PA	0V	15w-HD D	J5	7
SCL_RFA_TX	IO	Opto isolated logic	I2C Clock_TX		15w-HD D	J5	2
SCL_RFA_RX		Opto isolated logic	I2C Clock_RX		15w-HD D	J5	3
SDA_RFA_TY	IO	Opto isolated logic	I2C Data_TY		15w-HD D	J5	5
SDA_RFA_RY		Opto isolated logic	I2C Data_RY		15w-HD D	J6	6
EXT-CONVST	Out	Opto isolated logic	Start ADC conversion		15w-HD D	J5	8
-EXT_GATE	Out	Opto isolated logic	Enable connected amplifier		15w-HD D	J5	9
EXT-BSY	In	Opto isolated logic	ADC conversion busy		15w-HD D	J5	11
EXT-INT_MON	In	Opto isolated logic	Interlocks valid monitor		15w-HD D	J5	12
* Applies only when signals supported by connected PA							



11 Signal Timing Diagram

Applies to Image mode.

NOTE: For clarity, the 1.2usec latency between the External clock and the respective Output frequency point is not shown. This is a pipeline delay and does not impact on Image Clock rate.



12 J8 External reference (ERC)

iMS4- revD models employ a PLL to generate the system clock for the DDS chips, AD9958. By default, an internal 25MHz TCXO connects to the PLL reference clock input. Optionally, the user can provide an external reference clock on SMA, J8. Contact Isomet for guidance to enable this option.

The ERC input requires a sinusoidal clock input and is 50 ohm terminated .

Reference Clock:

Frequency:	Any multiple of 20KHz
Minimum	40KHz
Maximum	16MHz
Level:	50ohm input impedance
Minimum	0dBm (1mW)
Maximum	20dBm (100mW)



13 Software.

The core of the Software Development Kit is the C++ iMS library and API. All interaction with iMS hardware ultimately passes through this API. However, we have also provided a number of other software utilities and wrappers that allow you to use the iMS System at a higher level of abstraction.

Included in the SDK are:

- The core iMSLibrary binaries for a number of different platforms and toolsets.
- Accompanying C++ header files for application interface.
- iMSNET An experimental .NET assembly written in C# that wraps the core library and permits user application development in any .NET language targeting the .NET Framework
- ims_hw_server is a command line daemon type process that can handle all communication with an iMS system, decoupling it from user application business logic. A gRPC streaming interface connects the server to application software, either on the same host or across a network.
- iMS Studio is a full featured GUI front end application that can be used to create Images, Tone Buffers and Compensation Functions and play them on an iMS system. This is often a good starting point for users wishing to explore the capabilities of an iMS before starting development of custom software.**

The iMS software is available for download from http://www.isomet.com/ims4_sw.html

Depending on your computer select and run one of the following :

Isomet iMS SDK v 1.x.x Win7 Setup.exe

Isomet iMS SDK v 1.x.x Win10 Setup.exe

The software download also includes documentation and tutorials for setting up a project and connecting to the iMS. Note: these Tutorials are NOT specific to any practical AO device.

Please refer to **Quick Start Guide: Isomet iMS Studio** for instructions on the Isomet Windows GUI

The iMS software library and API has been written purely in native ANSI-C++ with some use of features introduced in C++11 (ISO/IEC 14882:2011), including the C++ Standard Library. There is no use of features associated with the updated C++14 specification.

Isomet will provide example projects applicable to the customer hardware configuration.

The Software Development Kits are regularly updated. Please check for Isomet website for updates.

a. Visual Studio Notes

	Visual Studio 2013 (v120)		Visual Studio 2015 (v140)	
	32-bit	64-bit	32-bit	64-bit
Microsoft Windows 2000/XP/Vista or earlier	✗	✗	✗	✗
Microsoft Windows 7 Professional	✓	✓	✓	✓
Microsoft Windows 8/8.1	⚠	⚠	⚠	⚠
Microsoft Windows 10 Professional	✗	✗	✓	✓

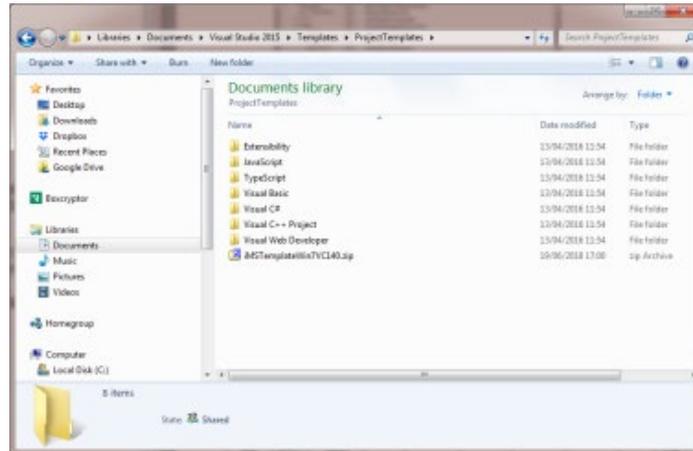
Table 1 Toolset Version Compatibility Table

b. Folder locations.

For ease of installation, a C++ console application template file is provided.

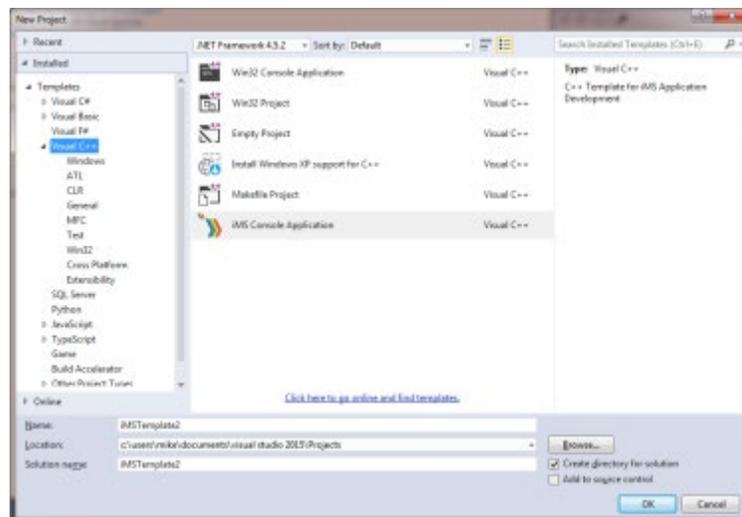
Copy the file *imSTemplateWin7VC140.zip* into the Visual Studio project templates folder e.g. C:.....Documents > Visual Studio 2015 > Templates > ProjectTemplates

DO NOT unzip



When starting *New Project* from Visual Studio, the *ims Console Application* will be offered Edit the project Location as required.

However Rename in VCP++ Solution Explorer window after Template project is started.



c. Adding C++ code to the project template

Please refer to the comments within the C++ template code and the ReadMe.txt file

The application includes the example code necessary for connection to the iMS4 (via selected ports) and files which are used to build a precompiled header (PCH) file; StdAfx.h, StdAfx.cpp

Add additional include files to *StdAfx.h*

```

StdAfx.h  X  iMSEncoderDemo.cpp
iMSEncoderDemo  (Global Scope)
1  // StdAfx.h : include file for standard system include files,
2  // or project specific include files that are used frequently, but
3  // are changed infrequently
4  //
5  //
6  #pragma once
7  // These are the API header files we will need
8  //
9  //
10 #include "ConnectionList.h"
11 #include "iMSSystem.h"
12 #include "SystemFunc.h"
13 #include "ImageOps.h"
14 #include "Compensation.h"
15 #include "SignalPath.h"
16 #include "ToneBuffer.h"
17 #include "SystemFunc.h"
18 #include "iMSTypeDefs.h"
19 #include "libxl.h"
20
21 #include <cstdio>
22 #include <cstdlib>
23 #include <sstream>
24 #include <fstream>
25 #include <thread>
26 #include <vector>
27 #include <conio.h>
28
29
30 // TODO: reference additional headers your program requires here
31
32

```

Referencing the default Source file (e.g. iMSTemplate.cpp)

User application code is added from line 111

```

iMSTemplate2.cpp  StdAfx.h
iMSTemplate2  (Global Scope)
99
100     if ((ch - '0') > 0 && (ch - '0') <= (int)(fullIMSList.size())) {
101         myIMS = fullIMSList[ch - '0'];
102         break;
103     }
104     std::cout << std::endl;
105
106     std::cout << "Connecting ... ";
107     myIMS->Connect();
108     std::cout << "OK" << std::endl;
109
110
111     // Application Code goes here
112     //
113
114
115
116     //
117     // CLEANUP
118     //
119
120     myIMS->Disconnect();
121     std::cout << "Press a key to exit..." << std::endl;
122     while (!_kbhit());
123
124     return 0;
125
126
127

```

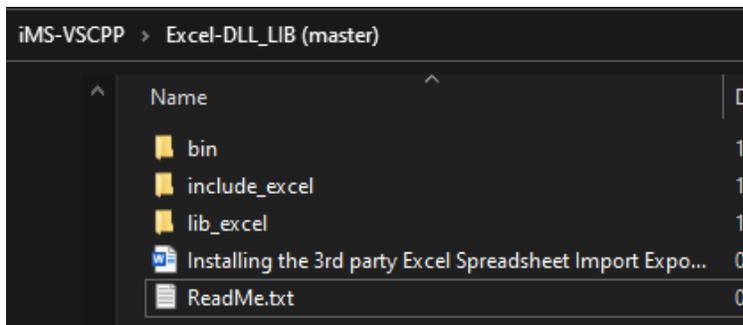
d. Installing the 3rd party Excel Spreadsheet Import Export function

Generating Compensation Tables (LUTs) and Image files in Excel can be convenient. Several routines exist to import data into C++. One such is from libxl.com. A licence key is required, and it is free to use. Add the following code prior to calling the LibXL functions.

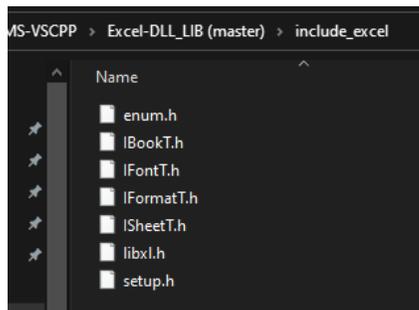
```
// call LibXL licence key
libxl::Book* ExcelBook = xlCreateBook();
ExcelBook->setKey(L"Michael Hillier", L"windows-222329040ec5ec046fb46767a7h1gej6");
```

To add this feature to your project

Create a folder Excel-DLL_LIB in the Projects folder and download associated files (contact Isomet)

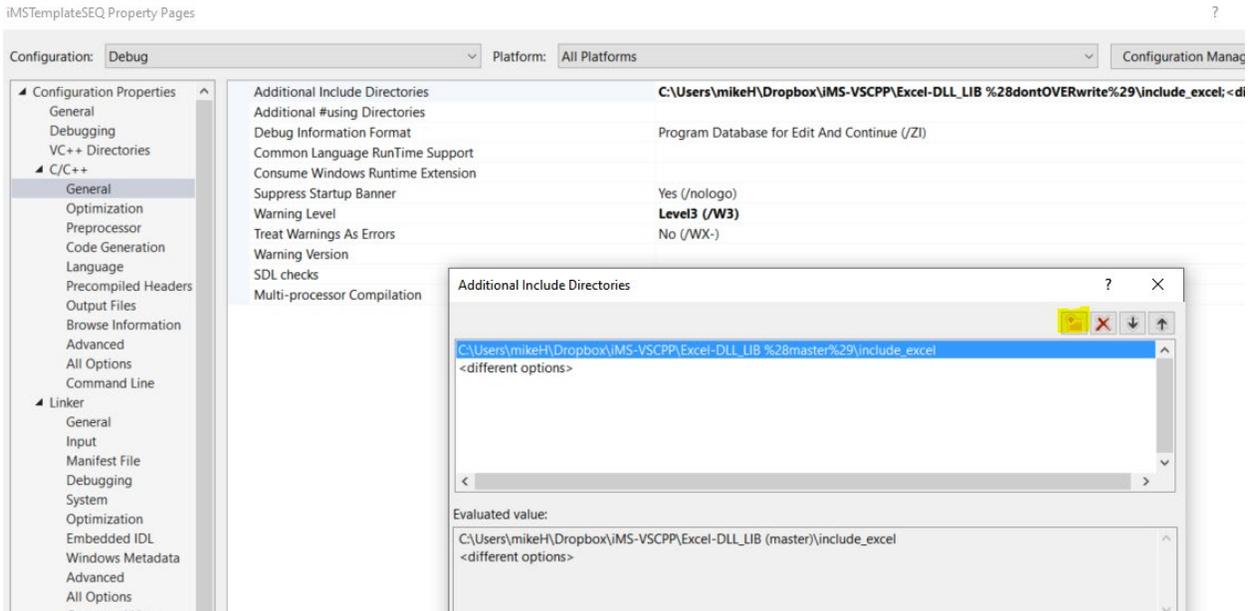


- Copy the include files from *include_excel* folder to MS VS installed folder
e.g. to *C:\Program Files (x86)\Microsoft Visual Studio 14.0\VC\include*



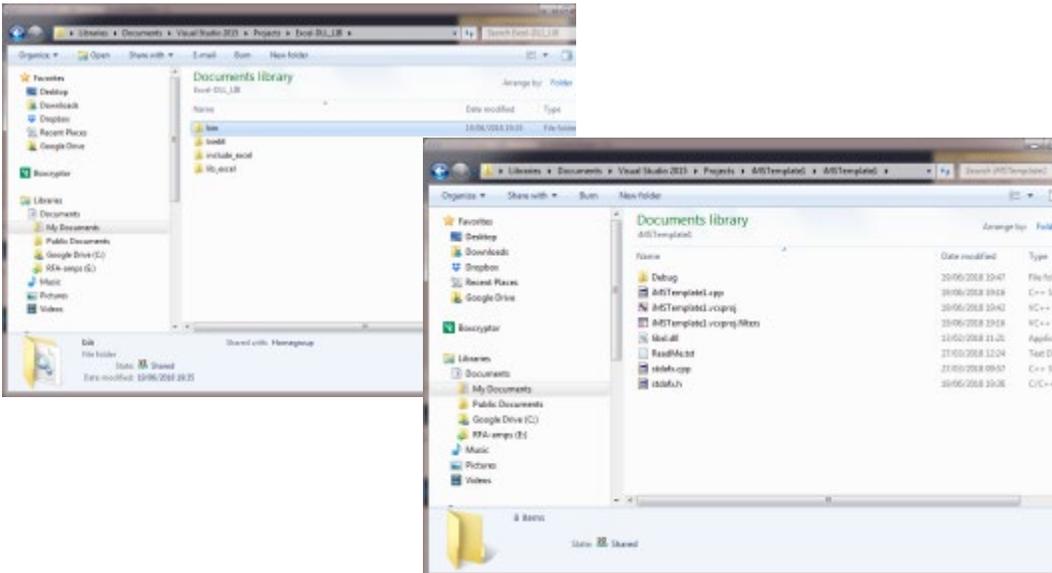
(Subsequently if using the Isomet template project, add additional include files to **StdAfx.h** only)

Add 'include_excel' to the *Additional Include Directory* under *C++ > General*.

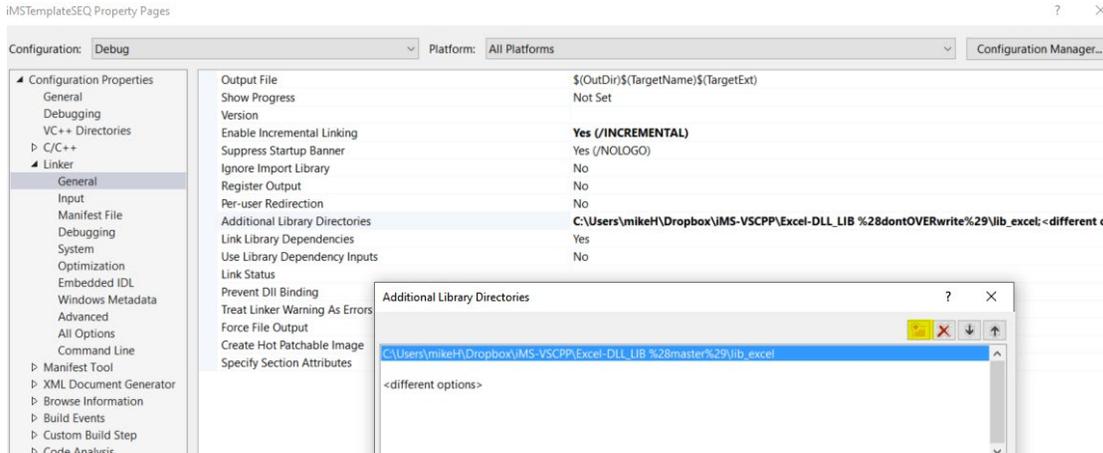


- Copy **libxl.dll** from > *Excel_DLL-LIB* > *bin* to the project folder you created.

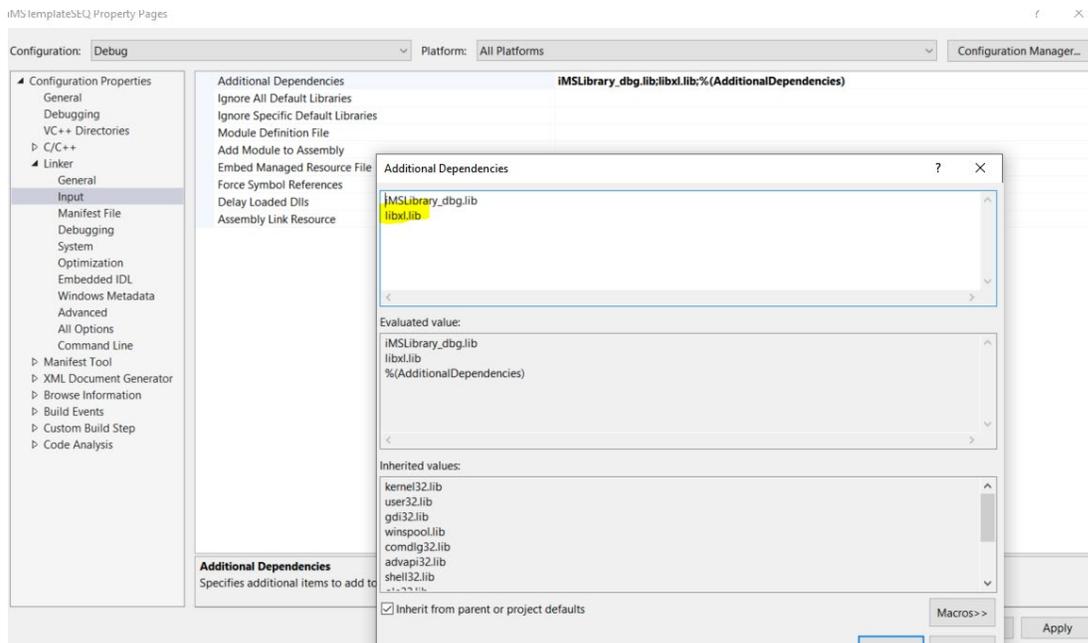
It must be in the same folder as the source file *.cpp.



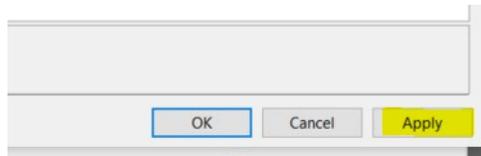
- Add the folder containing libxl.lib to the *Additional Library Dependencies* under *Linker > General*.



- Add libxl.lib to the *Additional Dependencies* under *Linker > Input*



- To implement the above , hit *Apply*





14 Direct programming of the DDS Synthesizer Chip.

For most applications, the use of the DDSscript function is not required (C++ only)

Use with CAUTION

The DDS IC that generates the RF signals can be manually programmed to access advanced features that wouldn't normally be available through the iMS API. To do this requires a detailed knowledge and understanding of the Analog Devices AD9958 Frequency Synthesiser IC and its register map.

If it is necessary to manually program the AD9958, a sequence of register writes can be generated (called a DDS Script) and stored in the Synthesiser Filesystem. The application software may then recall the script from the filesystem and execute it to commit the register writes to the AD9959. Please refer to DDSscript Class description in the SDK documentation.

REGISTER MAPS

Each register write is initialised with the name of the register as the first argument. (This is in the same abbreviated form as specified in the AD9958 datasheet).

Control Register Map

Register Name (Serial Addr)	Bit Range	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0 (LSB)	Default Value
Channel Select Register (CSR) (0x00)	[7:0]	Channel 1 Enable * (1 = On)	Channel 0 Enable *	Open	Open	Must be 0	Serial I/O mode Select [2:1] B2=1, B1=0		LSB first	0xF4 DO NOT CHANGE
Function Register 1 (FR1) (0x01)	[23:16]	VCO gain control	PLL divider ratio[22:18]				Charge pump Control [17:16]		0xD0	
	[15:8]	Open	Profile pin configuration (PPC) [14:12]			Ramp-up/down (RU/RD) [11:10]	Modulation level [9:8]		0x00	
	[7:0]	Reference clock input power-down	External power-down mode	SYNC_CLK disable	DAC reference power-down	Open [3:2]	Manual hardware sync	Manual sync	0x00	
Function Register 2 (FR2) (0x02)	[15:8]	All channels autoclear sweep accumulator	All channels clear sweep accumulator	All channels autoclear phase accumulator	All channels clear phase accumulator	Open [11:10]	Open [9:8]		0x20	
	[7:0]	Auto sweep sync enable	Multidevice sync master enable	Multidevice sync status	Multidevice sync mask	Open [3:2]	System clock offset [1:0]		0x00	

Defaults = Power -on hard coded DDSScript

* Channel enable bits do not require an I/O update to be activated. These bits are active immediately after the byte containing the bits is written. All other bits need an I/O update to become active.

These four channels enable bits are used to enable/disable any combination of the four channels. The default is all four enabled.



Channel Register Map

Register Name (Serial Addr)	Bit Range	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	
* Channel Function Register (CFR) (0x03)	[23:16]	Amplitude freq. phase (AFP) select [23:22]		Open [21:16]							0x00
	[15:8]	Linear sweep no-dwell	Linear sweep enable	Load SRR at I/O_UPDATE	Open [12:11]		Must be 0	DAC full-scale current		0x03	
	[7:0]	Digital power-down	DAC power-down	Matched pipe delays active	Autoclear sweep accumulator	Clear sweep accumulator	Autoclear phase accumulator	Clear phase Accumulator **	Sine wave output enable	0x00	
* Channel Frequency Tuning Word 0 (CFTW0) (0x04)	[31:24]	Frequency Tuning Word 0 [31:24]									0x00
	[23:16]	Frequency Tuning Word 0 [23:16]									N/A
	[15:8]	Frequency Tuning Word 0 [15:8]									N/A
	[7:0]	Frequency Tuning Word 0 [7:0]									N/A
* Channel Phase Offset Word 0 (CPOW0) (0x05)	[15:8]	Open [15:14]		Phase Offset Word 0 [13:8]						0x00	
	[7:0]	Phase Offset Word 0 [7:0]									0x00
Amplitude Control Register (ACR) (0x06)	[23:16]	Amplitude ramp rate [23:16]									N/A
	[15:8]	Increment/decrement step size [15:14]		Open	Amplitude multiplier enable	Ramp-up/down enable	Load ARR at I/O_UPDATE	Amplitude scale Factor [9:8]		0x13	
	[7:0]	Amplitude scale factor [7:0]									0xFF
* Linear Sweep Ramp Rate (LSRR) (0x07)	[15:8]	Falling sweep ramp rate (FSRR) [15:8]									N/A
	[7:0]	Rising sweep ramp rate (RSRR) [7:0]									N/A
* LSR Rising Delta Word (RDW) (0x08)	[31:24]	Rising delta word [31:24]									N/A
	[23:16]	Rising delta word [23:16]									N/A
	[15:8]	Rising delta word [15:8]									N/A
	[7:0]	Rising delta word [7:0]									N/A
* LSR Falling Delta Word (FDW) (0x09)	[31:24]	Falling delta word [31:24]									N/A
	[23:16]	Falling delta word [23:16]									N/A
	[15:8]	Falling delta word [15:8]									N/A
	[7:0]	Falling delta word [7:0]									N/A

** The clear phase accumulator bit is set to Logic 1 after a master reset. It self-clears or is set to Logic 0 when an I/O update is asserted.

* There are four sets of channel registers and profile registers, one per channel. The addresses of all channel registers and profile registers are the same for each channel. The channel enable bits (Control Register 0, CSR [7:4]) determine if the channel registers and/or profile registers of each channel are written to or not.



Profile Register Map

For clarity, only the MSB byte is shown for each Channel Word register.

Register Name	Bit Range	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0 (LSB)	Default Value
Channel Word 1 (CW1) (0x0A)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 2 (CW2) (0x0B)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 3 (CW3) (0x0C)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 4 (CW4) (0x0D)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 5 (CW5) (0x0E)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 6 (CW6) (0x0F)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 7 (CW7) (0x10)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 8 (CW8) (0x11)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 9 (CW9) (0x12)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 10 (CW10) (0x13)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 11 (CW11) (0x14)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 12 (CW12) (0x15)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 13 (CW13) (0x16)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 14 (CW14) (0x17)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A
Channel Word 15 (CW15) (0x18)	[31:0]	Frequency tuning word [31:0] or Phase word [31:18] or Amplitude word [31:22]								N/A

Each channel word register has a capacity of 32 bits (only 8 shown above).

If phase or amplitude is stored in the channel word registers, it must be first MSB aligned per the bit range.

File System

Once created, DDSScripts can be downloaded to the filesystem on the Synthesiser (they can only be committed to the AD9958 from the file system, they cannot be executed directly).

Create a DDSScriptDownload object initialised from the DDSScript and the attached iMS, then call the Program() function to transfer the contents. The function parameters assign a file name (max 8 chars) to the script stored in the Filesystem and indicate whether it should be executed at power-up (DEFAULT) or not (NON_DEFAULT). This second argument is optional, if not given, it will be set to NON_DEFAULT.

Note that only one script in the Filesystem can be set to DEFAULT.